REMARKS

Claims 1-27 are pending in this application. By this Amendment, claims 1, 3, 17 and 25 are amended. Support for the amendment is found in the specification, Fig. 8, for example. No new matter is added.

This reply is submitted as a complete response to the outstanding Office Action. Reconsideration of the application in view of the above amendments and following remarks is respectfully requested.

MATTERS OF FORM

The Office Action objects to the title. Applicant has amended the title to recite "A Semiconductor Phase Adjustment System Module". Accordingly, Applicant respectfully requests the withdrawal of the objection to the title.

The Office Action rejects claims 1-24 under 35 U.S.C. § 112, second paragraph. Specifically, claims 1-2 are rejected as being incomplete for omitting essential structural cooperative relationships. Additionally, claim 17 is rejected for lack of antecedent basis. Applicant has amended the claims to obviate this rejection. Accordingly, Applicant respectfully requests the withdrawal of the rejection under 35 U.S.C. § 112, second paragraph.

PATENTABLE SUBJECT MATTER

The Office Action rejects claims 1-3, 5, 15-18 and 21 under 35 U.S.C. § 102(b) over Kikukawa et al. (U.S. Patent No. 5,835,424). This rejection is respectfully traversed.

Applicant's independent claim 1 recites a module comprising, a semiconductor device, a phase adjustment circuit which receives a phase adjustment signal output

from said semiconductor device and a first clock supplied from an exterior of said module, and generates a second clock, and an output circuit that is provided in the semiconductor device and generates the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock.

Applicant's independent claim 3 recites a module comprising, semiconductor devices, one of which is a first semiconductor device that outputs a phase adjustment signal, a phase adjustment circuit which receives the phase adjustment signal output from said first semiconductor device and a first clock supplied from an exterior of said module, and generates a second clock, the second clock being supplied to the semiconductor devices, and a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted, the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock.

Kikukawa discloses a synchronous DRAM semiconductor memory for receiving and supplying data in synchronism with an external clock signal, wherein address-comparing circuits for redundancy judgment is applied. A first memory bank 10 and second memory bank 20 are connected to row predecoder 11/21, row redundancy judging circuit 12/22, and column redundancy judging circuit 13/33. An address buffer 51 receives an external address ADR to respectively supply the row and column addresses. An internal clock signal ICLK is provided with an internal column address

ICA. The internal clock signal ICLK is a signal formed from the internal clock signal CLK such that the internal clock signal ICLK has pulses and number corresponding to the data burst length. See col. 4, lines 1-39, for example. The row redundancy judging circuits are arranged to receive a row address given as the internal address IADR and to supply a row redundancy judging signal RRJ to the memory banks. Thus, for low speed or high speed mode operation, according to the external clock signal speed, the frequency of the external clocks input signal is divided to provide a sufficient time of judgment for each of the address comparing circuits.

Given the above disclosure of Kikukawa, it is readily apparent that Kikukawa is directed to an altogether different system and/or process than Applicant's claimed invention. In fact, Kikukawa does not contain any disclosure or suggestion relating to adjusting a phase of the second clock (ICLK) such as to fix a relative phase difference between the phase adjustment signal (ICA) and the first clock (CLK), as recited in Applicant's independent claims 1 and 3. Thus, in view of the above, Applicant respectfully submits that Kikukawa does not disclose or suggest all the claimed features of Applicant's invention.

Claim 2 depends from claim 1, and claims 5, 15-18 and 21 depend from claim 3. Accordingly, for at least the above reasons, Applicant respectfully requests the withdrawal of the rejection under 35 U.S.C. § 102(b) over Kikukawa.

The Office Action rejects claims 25-28 under 35 U.S.C. § 102(e) over Hashimoto (U.S. Patent No. 6,351,166). This rejection is respectfully traversed.

Applicant's independent claim 25 recites a system comprising, modules, a wiring board on which the modules are mounted, and a dummy output load line serving as

loads of dummy output data output from the modules, wherein the modules comprise a module including, semiconductor devices, one of which is a first semiconductor device that outputs a phase adjustment signal, a phase adjustment circuit which receives the phase adjustment signal output from said first semiconductor device and a first clock supplied from an exterior of said module, and generates a second clock, the second clock being supplied to the semiconductor devices, and a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted, the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference from the phase adjustment signal and the first clock.

Hashimoto discloses a semiconductor device having a timing-stabilization circuit for adjusting a phase of the synchronization clock signal. The output-timing adjustment operation is suspended during a time period when the data is output. However, notwithstanding the ability of Hashimoto to provide a phase-adjusted signal, Applicant respectfully submits that Hashimoto does not disclose the ability to have a plurality of semiconductor devices receiving a second clock, a phase adjustment circuit, wherein one of the semiconductor devices outputs a phase adjustment signal to the phase adjustment circuit.

For example, as explained in the Applicant's specification, beginning at page 9, line 25 - page 10, line 5, a plurality of memory devices 120 - 127 are provided. Only one of the memory device 123 is allowed to generate dummy output data (e.g., phase adjustment signal). The ability provide a phase adjustment signal from one of a

plurality of semiconductor devices "back" to the phase adjustment circuit is not disclosed in Hashimoto.

Hashimoto's phase adjustment signal comes from an "internal" dummy path via dummy output circuit 20, dummy output load 21, ESD 22, and dummy input circuit 19. Hashimoto provides an output signal to "non-illustrated" semiconductor devices connected to the output circuit/output node 11, however these semiconductor devices do not provide a phase adjustment signal back to the device of Hashimoto. Contrast Applicant's Fig. 7 signal line with Hashimoto's output 11. Therefore, Hashimoto does not disclose or suggest modules including semiconductor devices, one of which is a first semiconductor device that outputs a phase adjustment signal.

Thus, it is respectfully submitted, in view of the above, that Hashimoto does not disclose or suggest all the claimed features of Applicant's invention.

Claims 26-27 depend from claim 25. Therefore, for at least the above reasons, Applicant respectfully requests the withdrawal of the rejection under 35 U.S.C. § 102(e) over Hashimoto.

CONCLUSION

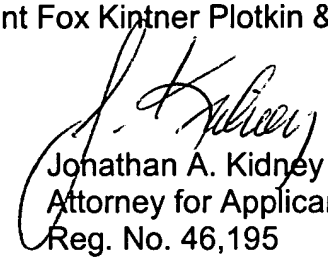
In view of the above remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance of claims is earnestly solicited. Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge

payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to client-matter number 100353-00064.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn



Jonathan A. Kidney
Attorney for Applicant
Reg. No. 46,195

Customer No. 004372
1050 Connecticut Ave. NW
Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6481
Fax: (202) 638-4810

JAK:ksm

Enclosures: Marked-Up Copy of Amended Specification
Marked-Up Copy of Amended Claims

MARKED-UP COPY OF AMENDED SPECIFICATION

Page 9, paragraph 8, beginning at line 25:

Fig. [1] 7 is a block diagram of a module according to a first embodiment of the present invention. A memory module 14 shown in Fig. 7 includes, on a wiring board 160, memory devices 120 - 127 having an identical structure, a PLL circuit (PLL1) 15 for an input clock, a PLL circuit (PLL2) 16 for an output clock, data input/output terminals DQ and a clock input terminal CLK. A positive power source voltage VCC is applied, as an external instruction signal, to a dummy output enable terminal of the memory device 123. The remaining memory modules 120 - 122 and 124 - 127 are supplied with a negative power source voltage (ground voltage) VSS via the respective dummy output enable terminal. Thus, only the memory device 123 is allowed to generate dummy output data, which will be described later. In the specification, clocks handled within the module are internal clocks.

Page 10, paragraph 3, beginning at line 27:

The PLL circuit 16 receives dummy output data, which is output from the memory device 123 via the dummy output terminal P2. Then, the PLL circuit 16 compares the phase of the dummy output data with that of the external clock. As will be described later, the memory device 123 is capable of generating dummy output data from the clock received via the dummy data output terminal P2. The timing of the clock used to output data is adjusted by the PLL circuit 16 so that the dummy output data and the external clock are pulled in phase. If the dummy output data has the same delay amount as the data output signal lines 24, the dummy output data and the output data at the data input/output terminal DQ are in phase. That is, the output data at the data

input/output terminal DQ is synchronized with the external clock. In that manner, the dummy output data functions as a phase adjustment signal.

MARKED-UP COPY OF AMENDED CLAIMS

1. (Once Amended) A module comprising:

a semiconductor device;

a phase adjustment circuit which receives a phase adjustment signal output from said semiconductor device and a first clock supplied from an exterior of said module, and [generating] generates a second clock [so that a phase adjustment signal output from the semiconductor device and a first clock have a predetermined phase relationship]; and

an output circuit that is provided in the semiconductor device and generates the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock.

3. (Once Amended) A module comprising:

semiconductor devices, one of which is a first semiconductor device that outputs a phase adjustment signal;

a phase adjustment circuit which receives the phase adjustment signal output from said first semiconductor device and a first clock supplied from an exterior of said module, and [generating] generates a second clock [so that a phase adjustment signal output from a first semiconductor device that is one of the semiconductor devices and a first clock have a predetermined phase relationship], the second clock being supplied to the semiconductor devices; and

a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted,

the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock.

17. (Once Amended) The module as claimed in claim 3, wherein:

the semiconductor devices including the first semiconductor device have an identical circuit configuration; and

the output circuit of the first semiconductor device [has an output circuit that] receives an external instruction that instructs the first semiconductor device to generate the phase adjustment signal.

25. (Once Amended) A system comprising:

modules;

a wiring board on which the modules are mounted; and

a dummy output load line serving as loads of dummy output data output from the modules, wherein the modules comprise a module including:

semiconductor devices, one of which is a first semiconductor device that outputs a phase adjustment signal;

a phase adjustment circuit which receives the phase adjustment signal output from said first semiconductor device and a first clock supplied from an exterior of said module, and generates a second clock, the second clock being supplied to the semiconductor devices; and

a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted,

the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference from the phase adjustment signal and the first clock.